REMARKS

Claims 3-7 and 9-32 were previously pending in this application. No claims are amended and no claims are canceled herein. No new claims are added herein. As a result, claims 3-7 and 9-32 are pending for examination with claims 11, 15, 24 and 30 being independent claims.

Summary of Telephone Conference with Examiner

Applicants thank Examiner Atala for her time and courtesy during the telephone interview conducted on April 16, 2009 with the undersigned. During the interview the parties discussed the Declaration and Exhibits submitted with the immediately preceding Response. The parties also discussed the commonality of the disclosure of U.S. Publication No. 2007/0217518 to Valmiki (hereinafter "Valmiki") and U.S. Patent No. 6,853,385 to MacInnis et al. (hereinafter "MacInnis"). Applicants pointed out that the Declaration and Exhibits are equally effective against both Valmiki and MacInnis. The Examiner indicated that a Response should be submitted to formally address the preceding.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 3-7 and 9-32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,678,002 to Frink et al. (hereinafter "Frink") in view of MacInnis and further in view of Valmiki. Applicants respectfully disagree and traverse this rejection for the reasons described below.

1. The Office Action Contains Legal Error by Ignoring the Applicants' Declaration

A Declaration of Lorne Trottier et al. under 37 C.F.R. §1.131, and supporting Exhibits A-E were submitted in the Amendment and Response filed on December 5, 2008 ("the December Response"). The Declaration and Exhibits provide detailed and comprehensive evidence of an actual reduction to practice of the subject matter of claims 3-7 and 9-32 prior to November 9, 1999, which is the earliest effective date of each of MacInnis and Valmiki. For example, see paragraphs 7 and 8 of the Declaration which identify a direct association between the evidence and the claimed subject matter.

Yet, the instant Office Action completely ignores the Declaration failing even to acknowledge its receipt let alone to give the Declaration any weight. Instead, the Office Action cites a new reference from the same patent family as MacInnis. That is, the Office Action introduces a newly-cited reference, Valmiki, having a Detailed Description which is substantially identical to the Detailed Description of MacInnis and having the same effective date as MacInnis, the very reference that the Declaration addressed in the December Response. Applicants respectfully assert that the Declaration must be accorded weight. (See MPEP 715.07 "the examiner must consider all of the evidence presented in its entirety, including the affidavits or declarations and all accompanying exhibits.") Further, Applicants assert that the evidence provided by the Declaration is more than sufficient to prove an actual reduction to practice which is earlier than the effective date of each of MacInnis and Valmiki.

The Priority information for MacInnis and Valmiki is illustrated below:

MACINNIS

Application	Continuity Type	Parent	Parent Filing Date
MacInnis	Continuation in Part of	U.S. Pat. No. 6,570,579	11/09/99
U.S. Pat. No. 6,570,579	Priority under 119(e)	U.S.S.N. 60/107,875	11/09/98
MacInnis	Priority under 119(e)	U.S.S.N. 60/170,866	12/14/99

VALMIKI

Application	Continuity Type	Parent	Parent Filing Date
Valmiki	Continuation	U.S. Pat. No. 6,636,222	08/18/00
U.S. Pat. No. 6,636,222	Continuation in Part of	U.S. Pat. No. 6,570,579	11/09/99
U.S. Pat. No. 6,570,579	Priority under 119(e)	U.S.S.N. 60/107,875	11/09/98
U.S. Pat. No. 6,636,222	Priority under 119(e)	U.S.S.N. 60/170,866	12/14/99

Applicants respectfully assert that: 1) the Detailed Description included in each of MacInnis and Valmiki is substantially identical; 2) the same Figures are provided in each of MacInnis and Valmiki; and 3) the effective date of each of MacInnis and Valmiki is identical. Thus, a Declaration effective to antedate MacInnis is equally effective to antedate Valmiki.

As explained in the December Response, the effective date of MacInnis concerning the subject matter of the pending claims is no earlier than November 9, 1999. The preceding is true because all of the priority applications listed above (except the '875 application) were filed on November 9, 1999 or later. The '875 application does not teach or suggest anything concerning "a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams, said graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams," as recited in claim 24, for example. In particular, the '875 application does not include Figure 1 of MacInnis or Valmiki or any description corresponding to the description in columns 5 and 60 of MacInnis (and paragraphs 83-85 of Valmiki) which are relied on in the Office Action for an alleged teaching of a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams. A copy of the '875 application was included with the December Response.

Thus, MacInnis and Valmiki are not available as prior art references concerning the subject matter of the pending claims, at least, because the Declaration provides evidence of an actual reduction to practice which is prior to the effective date of MacInnis and Valmiki. Applicants respectfully request that the Declaration be considered and accorded weight.

2. All of the Pending Claims Are Patentable Even in View of MacInnis and Valmiki

As indicated above, Applicants respectfully assert that MacInnis and Valmiki are unavailable as prior art references in view of the Declaration. In addition, Applicants respectfully assert that the instant Office Action does not provide a *prima facie* case of obviousness even in view of MacInnis and Valmiki, at least, because the asserted combination (Frink, MacInnis and Valmiki) does not teach or suggest all the limitations recited in the claims.

Applicants do not repeat the prior arguments concerning the deficiencies of the combination of Frink and MacInnis which were provided in the previous Responses (of July 23, 2007; February 11, 2008; and December 5, 2008) but note that they remain relevant in view of the current rejections because Valmiki does not provide description which was not already included in MacInnis. Accordingly, Applicants incorporate those arguments and remarks by reference herein.

For example, claim 24 recites "a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams, said graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams." All of the pending independent claims expressly recite a "graphics accelerator chip." (Emphasis added.) A graphics accelerator chip is a particular type of chip. The Office Action appears to treat any type of "graphics chip" as a "graphics accelerator chip" when referring to MacInnis and Valmiki. In doing so, the Office Action misses the fact that the cited references do not teach or suggest that a graphics accelerator of any type (a chip or otherwise) includes at least two video inputs for receiving at least two real-time uncompressed digital video streams as recited in claim 24. Such structure is absent from the cited references. Accordingly, claim 24 is patentable at least for that reason.

The mere teaching that a "graphics chip 10" includes "inputs 12 for receiving video signals 14" does not teach or suggest that any graphics accelerator can include a plurality of video inputs. (See MacInnis, Fig. 1 and Col. 5, lines 35-45.) The inconsistent and erroneous approach relied on in the Office Action is highlighted when page 4 of the Office Action ("MacInnis et al discloses a graphic processing system ... as seen in Figure 1") is compared with page 5 ("Valmiki et al further teaches a graphics accelerator chip ... as seen in Figure 1"). Figure 1 of MacInnis and Figure 1 of Valmiki are identical. Figure 1 does not illustrate a graphics accelerator chip nor does Fig. 1 in combination with the associated description teach or suggest a structure of a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams, as recited, for example, in claim 24.

Applicants respectfully assert that the preceding provides a positively recited structural limitation which is not taught or suggested by the references.

Instead, MacInnis dedicates approximately three columns to a description of the graphics accelerator 64 and its operation. (Col. 59, line 55 through col. 62, line 54.) In this substantial description, MacInnis does not provide any teaching or suggestion that the graphics accelerator 64 even receives a real time uncompressed video stream. Instead, MacInnis teaches a system in which video and graphics are processed in separate processing pipelines before being combined in a compositor 108. (See Fig. 4.) Thus, MacInnis employs "a dedicated processor" that includes "a memory for graphics data including pixels, and a coprocessor for performing vector type operations on a plurality of components of one pixel of graphics data." (Col. 59, lines 60-67, emphasis added.) As further explained in col. 60, "a graphics accelerator 64 receives commands from a CPU 22 and receives graphics data from main memory 28 through a memory controller 54." (Col. 60, lines 26-28, emphasis added.) Thus, MacInnis fails to teach or suggest that any real-time uncompressed video stream is supplied to a graphics accelerator let alone that at least two real-time uncompressed digital video streams are supplied to a graphics accelerator.

Further, even an addition, to the cited references, of a graphics accelerator chip having at least two video inputs for receiving at least two real-time uncompressed digital video streams (Applicants do not find the preceding in any of the cited references) does not teach or suggest all the limitations recited in claim 24. That is because the references also do not teach or suggest "a 2D graphics engine and 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams," as recited in claim 24. Claim 24 recites a novel and non-obvious relationship between the 2D graphics engine and 3D rendering engine and the at least two real-time uncompressed digital video streams. Applicants respectfully assert that the claims recite a pioneering structure and operation in which a graphics accelerator is employed to perform real time video editing on a plurality of uncompressed digital video streams. Such structure and operation is neither taught nor suggested by the cited references.

Claim 30 further highlights this deficiency in the *prima facie* case of obviousness even in view of MacInnis and Valmiki (which the Applicants assert cannot be properly applied as prior

art against the subject matter of the claims). Claim 30 recites a graphics accelerator chip including: a plurality of video inputs including: a first video input configured to receive a first real-time uncompressed digital video stream including a first plurality of video frames; and a second video input configured to receive a second real-time uncompressed digital video stream including a second plurality of video frames; a graphics input configured to receive graphics data; a 2D graphics engine and a 3D rendering engine each coupled to the first video input, the second video input and the graphics input, the 2D graphics engine and the 3D graphics engine configured to provide 2D and 3D functions, respectively, and to perform video editing in real time of the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream to generate an edited uncompressed digital video stream that includes at least a portion of one video frame of the first plurality of video frames, at least a portion of one video frame of the second plurality of video frames and the graphics data. (Emphasis added.)

In summary, MacInnis and Valmiki do not teach or suggest the above-recited structure. The mere teaching of editing video with a "graphics system" that also includes a "graphics accelerator" does not teach or suggest that a "graphics accelerator" of any type can include a 2D graphics engine and the 3D graphics engine configured to provide 2D and 3D functions, respectively, and perform video editing in real time of the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream to generate an edited uncompressed digital video stream that includes at least a portion of one video frame of the first plurality of video frames, at least a portion of one video frame of the second plurality of video frames and the graphics data. Thus, the cited references alone or in proper combination do not teach or suggest the preceding because the recited structure is absent from the cited references.

For all of the above reasons, Applicants respectfully assert that none of Frink, MacInnis or Valmiki alone or in proper combination teach or suggest all the limitations recited in independent claims 11, 15, 24 and 30. Each of claims 3-7, 9, 10, 12-14, 16-23, 25-29 and 31-32 depend from one of the allowable independent claims. Accordingly, reconsideration and withdrawal of the rejections of claims 3-7 and 9-32 under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

In view of the foregoing remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this response, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an accompanying payment, please charge any deficiency to Deposit Account No. 50/2762, M1073-700719.

Respectfully submitted,
Lorne Trottier et al., Applicants

By: /Robert V. Donahoe/

Robert V. Donahoe, Reg. No. 46,667
LOWRIE, LANDO & ANASTASI, LLP
One Main Street
Cambridge, Massachusetts 02142
United States of America
Telephone: 617-395-7000
Facsimile: 617-395-707

May 6, 2009